UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/564,293	01/10/2006	Gunnar Wetzker	NL 030813	6995

65913 7590 06/05/2009

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
GILES, EBONI N	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
06/05/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/564,293	WETZKER ET AL.	
	Examiner	Art Unit	
	EBONI GILES	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9, 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 January 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. This office action is in response to communication filed on 4/10/09. Claims 1-11 are pending in this application of which Claim 10 is cancelled and Claim 11 is new.

2. Applicant's arguments with respect to claims 1-9 and 11 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication 2004/0057534 to Masenten et al. ("Masenten") in view of U.S. Patent Publication 2004/0210801 to Prasad et al ("Prasad").

Regarding Claim 1, Masenten discloses "a receiver comprising a receiving stage that receives frequency signals; a mixing stage coupled to the receiving stage that generates converted frequency signals, a modulating stage coupled to the mixing stage that delta-sigma modulates the converted frequency signals; a filtering stage coupled to the modulating stage that filters the delta-sigma modulated converted frequency signals," where, in a third embodiment, the receiver includes an integrated low noise amplifier (LNA) which may utilize one broadband or multiple narrow band low noise amplifiers for amplifying received

RF signals...The output of the active LNA is inputted to an in-phase (I)-path mixer and quadrature (Q)-path mixer, each of whose function is to translate the center frequency of the desired RF signal by a local oscillator frequency, f_{LO}, to an intermediate frequency, f_{IF} (¶0030, Fig. 3, elements 10, 110, 120A, 120B) and further discloses in a fourth embodiment where the output of each mixer is coupled to a delta-sigma modulator respectively through Node 1. Node 1 is implemented as an IF filter that provide both a tuned output for the corresponding mixer and a bandpass centered at the IF frequency for the first stage of the corresponding delta-sigma modulator (¶ 0029, 0034, Fig. 4a, elements 120A, 120B, 130A, 130B, 140A, 140B).

Masenten does not expressly disclose "wherein the filtering stage comprises a decimator receiving an output signal from a time-control loop having a loop quantizer and a loop filter.

Prasad teaches a delta-sigma analog-to-digital converter (ADC) where each delta-sigma modulator comprises a summer, low pass filter, quantizer and DAC in a delta-sigma feedback loop. The outputs from the delta-sigma modulators are each passed through a digital decimation filter which reduces the sample rate. Delta-sigma modulators sample the analog input signals at an oversampling rate and output digital data based on the quantization at the oversampling rate (¶ 0014-0016, Fig. 1, elements 100, 102, 104, 105, 106, 107). The delta-sigma feedback loop would be operable as the claimed timing control loop since it adjusts the re-sampling instants of the ADC.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the receiver of Masenten with the decimation filter of Prasad. The suggestion/motivation would have been in order to acquire and track the timing of a given signal instance.

Regarding Claim 2, Masenten and Prasad disclose a receiver as recited in Claim 1 and further discloses that the modulating stage comprises a delta-sigma modulator comprising a low-pass filter; a quantizer coupled to the low-pass filter; and a digital-to-analog converter for feeding back an output of the quantizer to an input of the low-pass filter," where the output of each delta-sigma modulators is coupled to a decimation filter. Each decimation filter filters and decimates the output signal from the respective delta-sigma modulator to forma high resolution digital signal at a sampling rate where MD is the decimation ratio of the decimation filter. The decimation filter divides down the sampling rate of the digital signal by MD. Each decimation filter has a lowpass frequency response (¶ 0036-0038, Fig 6A-6C, elements 140A, 140B, 150A, 150B).

Regarding Claim 5, Masenten and Prasad disclose a receiver as recited in Clam 1 and Masenten further discloses that "the mixing stage comprises a mixer and the modulating stage comprises a delta-sigma modulator," where the mixers decompose the received signal into in-phase and quadrature phase components. The I mixer outputs the in-phase component of the received signal at the IF and the Q mixer outputs the quadrature component of the received signal at the IF (¶ 0032, Fig. 4a, elements 120A and 120B) and further discloses that the delta-

sigma modulator includes a lowpass filter for a follow-on Node within the delta-sigma modulator. The bandpass filters of Node 1 and the lowpass filter for the follow-on Node result in both a signal transfer function (STF) and noise transfer function with a bandpass transfer function centered at the IF frequency. This provides rejection of DC and 1/f noise components from the respective mixer and also provides IF pre-filtering to attenuate signals outside of the channel bandwidth of the desired signal (¶ 0035, Fig. 4a, elements 140A, 140B).

Regarding Claim 6, Masenten and Prasad disclose a receiver as recited in Claim 1 and Masenten further discloses in a fifth embodiment that the receiver may utilize one broadband DLNA to amplify both frequency bands…the differential output of the DLNA is coupled to both the in-phase mixer and the quadrature mixer. The in-phase mixer receives a differential in-phase local oscillator signal and the quadrature mixer receives a differential quadrature local oscillator signal from the clock generation and distribution circuit. The output of the I mixer is coupled to the I delta-sigma modulator via the I-path IF filter and the output of the mixer is coupled to the Q delta-sigma modulator via the Q-path IF filter (¶ 0046, Fig. 5, elements 110, 120A, 120B, 122B, 130A, 130B, 140A, 140B).

Regarding Claim 7, Masenten discloses "a system comprising a transmitter and a receiver," where high frequency signals are received through an antenna and inputted to a duplexer…The duplexer couples the receive signal to the receiver and couples transmit signals from the transmitter to the antenna (¶

0026, Fig. 1, elements 10, 20, 22, 23, 25). The receiver is drawn to the apparatus recited in Claim 1 as taught by Masenten and Prasad and rejected for the same reasons of obviousness above.

Process claim 8 is drawn to the method of using the corresponding apparatus claimed in claim 1. Therefore, process claim 8 corresponds to apparatus claim 1and is rejected for the same reasons of obviousness above.

As to Claim 9, they are rejected for the same reasons indicated above because they recite similar limitations claimed in Claim 1.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Pub. 2004/0057534 to Masenten et al. ("Masenten") in view of U.S. Patent Publication 2004/0210801 to Prasad et al ("Prasad") as applied to claim 2 above and in view of US Patent 7,194,036 to Melanson.

Regarding Claim 3, Masenten and Prasad disclose a receiver as recited in Claim 2.

Masenten and Prasad do not expressly disclose that the low-pass filter comprises a time-continuous filter.

Melanson discloses that "the low-pass filter comprises a time-continuous filter," where the first delta-sigma modulator has a low-pass STF (signal transfer function) defined by a complex set of poles (Col. 6, lines 15-16) where a signal transfer function with a set of poles is indicative of a time-continuous filter.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Pub. 2004/0057534 to Masenten et al. ("Masenten") in view of U.S. Patent

Publication 2004/0210801 to Prasad et al ("Prasad") as applied to claim 1 above and in further view of US Patent 7,130,327 to Robinson et al. ("Robinson").

Regarding Claim 4, Masenten and Prasad disclose a receiver as recited in Claim 1.

Masenten and Prasad do not expressly disclose a further mixing and filtering stage.

Robinson does expressly disclose "a further mixing stage coupled to the filtering stage for generating baseband signals; and a further filtering stage coupled to the further mixing stage for channel selective filtering the baseband signals," where the filter is operative to mitigate quantization noise and noise that has been shifted or shaped to out-of-band frequencies by the delta-sigma modulation implemented by the modulator. The filter output signal can be passed to an amplifier operative to amplify the selected signal pattern to provide an output signal at a desired level. The amplified signal can be provided as a local oscillator signal to drive a mixer such that the signal operates as a carrier frequency for transmission of wireless communication signals or for up or down conversion in a transceiver (Col. 8, lines 18-28).

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Pub. 2004/0057534 to Masenten et al. ("Masenten") in view of U.S. Patent Publication 2004/0210801 to Prasad et al ("Prasad") as applied to claim 1 above and in view of U.S. Patent 6,225,928 to Green.

Regarding Claim 4, Masenten and Prasad disclose a receiver as recited in Claim 1.

Masenten and Prasad do not expressly disclose an adder, an inverse z block or a gain block.

Green teaches that the loop filter further comprises: an adder that combines a detected signal with a feedback signal, thereby producing a sum; an inverse z block that receives the sum and produces a feedback signal; a gain block that processes the feedback signal (Col. 5, line 66 – Col. 6, line 34, Fig. 3, elements 206, 220, 222, 310, 312, 314, 316, 318, 320, 322, 324) where a delta-sigma ADC is described that comprises a complex bandpass loop filter with a transfer function, H(z). The in-phase and quadrature signals are received by the adder which subtracts them from a feedback signal. The output signals are provided to the complex loop filter for quantization. The in-phase and quadrature phase signals having a desired gain generate a feedback signal. The quantization noise is removed by passing it through decimation filters subsequent to the ADC. Green further discloses producing the output signal that is sent to the loop quantizer to control the decimator (Col. 13, lines 34-57, Fig. 10, elements 208, 1014, 1020, 1022, 1028, 1032, 1036, 1040) where the power estimation circuitry receives real (I) and imaginary (Q) output signals from the decimation filters, control circuitry receives power estimation signal and produces gain control signals which respectively control input and output variable gain blocks located in the ADC input and output imaginary paths.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the receiver of Masenten and Prasad with the loop filter of Green. The suggestion/motivation would have been in order to automatically detect and compensate for mismatches in the delta-sigma ADC (Col. 13, lines 34-35).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EBONI GILES whose telephone number is (571)270-7453. The examiner can normally be reached on 7:30 AM - 5 PM, M-F, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ EBONI GILES/
Examiner, Art Unit 2611

/Mohammad H Ghayour/
Supervisory Patent Examiner, Art Unit 2611